IN THE SPECIFICATION:

Please replace paragraph number **[0001]** with the following rewritten paragraph:

[0001] Cross-Reference to Related Applications: This application is a continuation of application Serial No. 09/506,205, filed February 17, 2000, ~~pending,~~ now U.S. Patent 6,471,780, issued October 29, 2002, which is a continuation of application Serial No. 09/041,913, filed March 13, 1998, pending.

Please replace paragraph number **[0034]** with the following rewritten paragraph:

[0034] Temperature variation according to the process of the present invention may be effected by altering one or more characteristics of the power that is required by a heat generating source, such as a conventional furnace or a rapid thermal processing system. Various characteristics of the power that may be altered in order to effect temperature variation include frequency, amplitude and phase. Similarly, multiple power frequencies may be summed. Altering such characteristics of the heat-generating power facilitates creation of temperature variations of virtually any profile, as may be illustrated by a line graph wherein temperature is plotted over time. Alternatively, the temperature variation of the process of the present invention may be effected by setting the process chamber to a predetermined, fixed temperature profile, which is also referred to as a temperature set point profile. A feedback control system of the type known in the art may be employed to alter the amount of power that is input into the process chamber in order to increase, maintain, or reduce the amount of heat that is generated in the process ~~chamber,~~ chamber and thereby substantially emulate the temperature set point profile.

Please replace paragraph number **[0037]** with the following rewritten paragraph:

[0037] The first embodiment of the process is particularly useful for enhancing the uniformity of materials that, under steady state reaction chamber temperature conditions, form thicker layers at the center region of a semiconductor wafer than at the edge region of the same due to a higher reaction rate at the center region than at the edge region since, in some layer formation processes, fewer reactants are available at the edge region than at the center region of a

semiconductor wafer, which may result in the formation of a layer with a ~~"convex" or~~ "convex" or "dome" (i.e., inverted "bowl" or "dish")~~-shaped~~ -shaped contour. Thus, the process of the present invention is useful for preventing the "convex" or "dome" (i.e., inverted "bowl" or "dish")~~-shaped~~ -shaped contours of layers that are typically formed by many conventionally employed processes which deposit or grow layers on semiconductor wafers under steady state temperature conditions. As explained previously, such non-uniformities are typically caused by the differential depletion of reactants, or the creation of reactant gradients, over the surface of the semiconductor wafer.

Please replace paragraph number **[0038]** with the following rewritten paragraph:

[0038] The formation of a doped amorphous silicon layer of substantially uniform properties is exemplary of the first embodiment of the process of the present invention. Typical conventional doped amorphous silicon deposition techniques, such as the exemplary process that is disclosed in United States Patent 4,963,506 (the "'506 Patent"), which issued to Hang M. Liaw, et al. on October 16, 1990, the disclosure of which is hereby incorporated by reference in its entirety, occur under steady state conditions within a reaction chamber that has been heated to between about 500° C. and 600° C. In contrast, the deposition of doped amorphous silicon in accordance with the first embodiment of the present invention occurs while the reaction chamber temperature is being increased to about 600° C. First, a semiconductor wafer upon which the doped amorphous silicon layer is to be formed is placed into a reaction chamber while the temperature within the chamber is held at "idle" (e.g., a temperature of about 500° C.). The temperature within the reaction chamber is then increased. As the reaction chamber reaches a desirable initial deposition temperature (e.g., about 525° C. for doped amorphous silicon), the appropriate, conventionally employed reactants are introduced therein. The rate at which the reaction chamber temperature is subsequently increased and the amount of the temperature increase is dependent upon several factors, including without limitation the specific type of material that is being deposited, the desired layer properties and the desired level of layer uniformity. The introduction of reactants into the reaction chamber continues until the

temperature within the reaction chamber reaches a desired terminal deposition temperature (e.g., about 500° C. to 550° C. for doped amorphous silicon), at which temperature the introduction of reactants is stopped. Subsequently, the temperature within the reaction chamber is decreased to the "idle" temperature and the semiconductor wafer may be removed therefrom.

Please replace paragraph number **[0039]** with the following rewritten paragraph:

[0039] For the purpose of comparison, a layer of doped amorphous silicon was formed upon a semiconductor wafer in accordance with a conventional steady state deposition technique while the semiconductor wafer was being rotated. The doped amorphous silicon layer had a "convex" or "dome"~~-shaped~~ -shaped contour, indicating that the doped amorphous silicon layer is thicker at the center region of the semiconductor wafer than at the edge region of the same. The doped amorphous silicon layer that was deposited by a prior art technique varied about 35Å from its thickest measured point (1015.81Å), near the center region of the semiconductor wafer, to its thinnest measured point (979.33Å), near the wafer's edge region, which is a variation of about 3.5% from the median thickness (about 1002Å) of the layer; thus, the standard deviation of the variation in thickness was about 1.2%.

Please replace paragraph number **[0040]** with the following rewritten paragraph:

[0040] In contrast, a doped amorphous silicon layer that was formed on a semiconductor wafer in accordance with the first embodiment of the inventive process, as explained above, exhibited a more uniform thickness than that of the conventional technique described in the preceding paragraph, as evidenced by the lack of an inverted "bowl" or "dish" ~~shaped~~ -shaped contour. Stated in relative terms, the doped amorphous silicon layer varied only about 8Å from its thickest measured point (1003.72Å) to its thinnest measured point (995.65Å), which is a variation of only about 0.8% from the median thickness (1001.20Å) of the layer; thus, the standard deviation of the variation in thickness was only about 0.25%. The doped amorphous silicon layer that was formed in accordance with the first embodiment of the inventive process had about one-fifth to about one-sixth the variation in thickness of the doped amorphous silicon

layer as a doped amorphous silicon layer of similar overall thickness that was deposited under prior art steady state temperature conditions.

Please replace paragraph number **[0044]** with the following rewritten paragraph:

[0044] The second embodiment of the inventive process is particularly useful for facilitating the formation of layers of substantially uniform properties from materials that, under steady state temperature conditions, form thinner layers at the center region of a semiconductor wafer than at its edge region. Thus, the second embodiment of the process is useful for preventing the formation of layers having concave "bowl" or "dish"~~-shaped~~ -shaped contours, which may occur when conventional techniques are employed.

Please replace paragraph number **[0046]** with the following rewritten paragraph:

[0046] FIGs. 4 and 5 are 49 point contour maps of semiconductor wafers bearing thick (i.e., 1,800Å to 2,000Å) silicon nitride layers. The contour map of FIG. 4 illustrates the thickness of a silicon nitride layer that has been formed upon a semiconductor wafer in a hot wall furnace by conventional steady state temperature deposition techniques. The silicon nitride layer shown in FIG. 4 has a "bowl" or "dish"~~-shaped~~ -shaped contour, which is typically caused by reactant gradients over the surface of a semiconductor wafer. As noted previously, when conventional techniques are employed which utilize steady state temperatures throughout the reaction chamber, the reaction rate of the edge region of a semiconductor wafer is higher than the temperature of the center region of the same. Additionally, it is known in the art that thicker layers of some materials form upon the higher temperature regions of a semiconductor wafer than upon the lower temperature regions thereof. Consequently, the use of steady state reaction temperatures throughout a deposition process may result in the formation of a silicon nitride layer having non-uniform properties due to the generation of reactant gradients thereabove. As illustrated by FIG. 4, the layer is thicker at the edge region of the semiconductor wafer than at its center region. The thickness of the silicon nitride layer varied, from its thinnest measured point (1,808.59Å) to its thickest measured point (1,874.90Å), by about 66Å, which is about 3.6% of the

total average layer thickness (1,833.47Å); thus, the standard deviation in layer thickness was about 1.1%.

Please replace paragraph number **[0047]** with the following rewritten paragraph:

[0047] In contrast, FIG. 5 is a contour map which depicts the thickness of a silicon nitride layer that has been formed upon a semiconductor wafer in accordance with the second embodiment of the process of the present invention (i.e., during a cool-down phase). The silicon nitride layer of FIG. 5 has a more uniform thickness than that of FIG. 4. The silicon nitride layer varied about 48Å from its thickest measured point (1,859.97Å) to its thinnest measured point (1,811.57Å), which is a variation of about 2.6% from the median thickness (1,836.30Å) of the layer; thus, the standard deviation of the variation in thickness was only about 0.75%. Moreover, the thickness of the silicon nitride layer depicted in FIG. 5 does not create the ~~bowl shaped~~ bowl-shaped contour of FIG. 4, indicating ~~that,~~ that when the process of the present invention is employed in order to form a silicon nitride layer upon a semiconductor wafer, the rate at which such a layer is formed on the edge region of the semiconductor wafer is not significantly higher than the rate at which a layer is formed on the center region of the same.

Please replace paragraph number **[0056]** with the following rewritten paragraph:

[0056] Oscillation of the temperature within the reaction chamber may also be effected during a so-called "steady ~~state",~~ state," or "conventional" anneal phase, which is also referred to as a substantially steady state temperature trend. As in the heat-up phase, oscillation, fluctuation, or intermittent variation of the temperature within the reaction chamber maintains a substantially uniform temperature over the surface of a semiconductor wafer during the "conventional" anneal phase. FIG. 8 is a line graph which illustrates the temperature within the reaction chamber plotted over time during a "conventional" anneal phase. Although the graph line is saw tooth configured, as explained previously, each temperature increase is not necessarily followed by a decrease in temperature. Similarly, other oscillating heat-up patterns and less predictable variations in the temperature of the surrounding environment during the

"conventional" anneal phase are also within the scope of the present invention. During the "conventional" anneal phase, the temperature may remain within a predetermined range.

Please replace paragraph number **[0063]** with the following rewritten paragraph:

[0063] An exemplary material layer formation system 16, which is depicted in FIG. 12, includes a reaction chamber 20 with a heating element 22 therein. System 16 may also include a temperature sensor 17, or feedback system, of a type known in the art. Temperature sensor 17 is at least partially located within reaction chamber 20 so as to facilitate measurement of the temperature within reaction chamber 20 or of various portions of a semiconductor wafer 24 or other substrate within reaction chamber 20. Semiconductor wafers 24a, 24b and 24c upon which a material layer is to be formed are positioned on a platen 23 in reaction chamber 20. Platen 23 may be rotated by way of a rotator 25. Reaction chamber 20 is heated to a desired temperature by inputting power into heating element 22. As the temperature within reaction chamber 20 increases, the temperature of each of semiconductor wafers 24a, 24b and 24c increases. ~~An edge heater~~ Heater 21 may also be positioned within reaction chamber 20 so as to increase the temperature of at least an edge of one or more semiconductor wafers 24 or other substrates located in reaction chamber 20. When the temperature of reaction chamber 20 reaches a first, or initial anneal, temperature, matter 26 of a type that will promote the formation of a material layer upon each of semiconductor wafers 24a, 24b and 24c is introduced into reaction chamber 20 through an inlet 28. Preferably, the introduction of matter 26 into reaction chamber 20 is continued until the reaction chamber reaches a second, or terminal anneal, temperature.